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TITLE

INTEGRATED CIRCUIT BTSC ENCODER

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RELATED APPLICATIONS

[001] This patent application claims priority from U.S. Provisional Patent Application serial number 60/495,509, entitled “Integrated Circuit BTSC Encoder” filed on August 14, 2003.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[002] The present invention is directed in general to communication systems. In one aspect, the present invention relates to a method and system for digitally encoding audio signals used in the broadcast of stereophonic audio signals for use in television and cable broadcasting. In a further aspect, the present invention provides an integrated circuit system for modulating an audio signal using digital BTSC stereo encoding techniques.

2. Related Art

[003] Existing television (TV) sets typically can process a variety of input signal types. However, older TV models may only have a Radio Frequency (RF) input. When using a Set Top Box (STB) to create a video source, a method is needed to get the video signal to the TV. The method used is to modulate the baseband signal to a selectable television channel. For example, North American STBs often modulate to the assigned Channel 3 or Channel 4 Radio Frequencies (RFs). The modulation is typically performed using analog techniques, via discrete components. The prior art approach to implementing the interface to a display requiring an RF modulated input signal has typically been to include these discrete components on a board that interfaces to an output

port of a device. This has proven to be a highly expensive endeavor as a relatively large amount of cost is associated with the RF input interface.

[004] There are additional drawbacks associated with conventional STB systems. For example, encoded stereo audio signals transmitted to a conventional STB system are typically received and decoded by stereo audio/video (A/V) components connected directly to the program source. Where A/V components are daisy-chained through a coaxial connector with a conventional STB (cable, television or satellite), only the first device to derive left and right audio in the chain receives stereo audio via the coaxial connector, and all remaining devices that have only decoding circuitry connected only by coaxial cable receive monaural sound. Thus, conventional STB systems provide only limited audio signal processing capabilities for distributing decoded audio signal information to television sets associated with the STB.

[005] An example of a conventional system is a STB cable television receiver system for decoding and distributing BTSC stereo encoded audio signals to associated television sets. In such conventional systems, a radio frequency modulator might be included for modulating the decoded audio signal for output from the STB. Such modulators might include some simple signal processing, such as signal preemphasis processing, but prior STB systems have not included on-chip standards-based stereo encoding of the audio signals prior to distribution to associated audio playback devices. In particular, prior STB systems have not included on-chip BTSC encoding of audio signals. As will be appreciated by those skilled in the art, the BTSC encoding standard for encoding stereo signals was adopted by the Federal Communications Commission (FCC). This standard is also referred to as the Multichannel Television Sound (MTS) Transmission and Audio Processing Requirements for the BTSC System – OET-60. This is an example of a standard which permitted television programs to be broadcast and received with bichannel audio, e.g., stereophonic sound. Similar to the definition of stereo for FM radio broadcast, MTS defined a system for enhanced, stereo audio for television broadcast and reception. Also known as BTSC stereo encoding (after the Broadcast Television System Committee (BTSC) that defined it), the BTSC transmission methodology is built around the concept of companding, which means that certain

aspects of the incoming signal are compressed during the encoding process. A complementary expansion of the signal is then applied during the decoding process.

[006] The original monophonic television signals carried only a single channel of audio. Due to the configuration of the monophonic television signal and the need to maintain compatibility with existing television sets, the stereophonic information was necessarily located in a higher frequency region of the BTSC signal, making the stereophonic channel much noisier than the monophonic audio channel. This resulted in an inherently higher noise floor for the stereo signal than for the monophonic signal. The BTSC standard overcame this problem by defining an encoding system that provided additional signal processing for the stereophonic audio signal. Prior to broadcast of a BTSC signal by a television station, the audio portion of a television program is encoded in the manner prescribed by the BTSC standard, and upon reception of a BTSC signal, a receiver (e.g., a television set) then decodes the audio portion in a complementary manner. This complementary encoding and decoding ensures that the signal-to-noise ratio of the entire stereo audio signal is maintained at acceptable levels.

[007] Figure 1 is a block diagram of the front end portion of an analog BTSC encoding system 100, as defined by the BTSC standard. Encoder 100 receives left and right channel audio input signals (indicated in Figure 1 as "L" and "R", respectively) and generates a conditioned sum signal and an encoded difference signal. It should be appreciated that, while the system of the prior art and that of the present invention is described as useful for encoding the left and right audio signals of a stereophonic signal that is subsequently transmitted as a television signal, the BTSC system also provides means to encode a separate audio signal called SAP (Second Audio Program), e.g., audio information in a different language, which is separated and selected by the end receiver. Further, noise reduction components of the BTSC encoding system can be used for other purposes besides television broadcast, such as for improving audio recordings.

[008] System 100 includes an input section 110, a sum channel processing section 120, and a difference channel processing section 130. Input section 110 receives the left and right channel audio input signals and generates a sum signal (indicated in Figure 1 as "L+R") and a difference signal (indicated in Figure 1 as "L-R"). It is well

known that for stereophonic signals, the sum signal $L+R$ may be used by itself to provide monophonic audio reproduction and it is this signal that is decoded by existing monophonic audio television sets to reproduce sound. In stereophonic receivers, the sum and difference signals can be added to and subtracted from one another to recover the original two stereophonic signals (L) and (R). Input section 110 includes two signal adders 112, 114. Adder 112 sums the left and right channel audio input signals to generate the sum signal, and adder 114 subtracts the right channel audio input signal from the left channel audio input signal to generate the difference signal.

[009] To accommodate transmission path conditions for television broadcasts, the difference signal is subjected to additional processing than that of the sum signal so that the dynamic range of the difference signal can be substantially preserved as compared to the sum signal. More particularly, the sum channel processing section 120 receives the sum signal and generates the conditioned sum signal. Section 120 includes a 75 μ s preemphasis filter 122 and a bandlimiter 124. The sum signal is applied to the input of filter 122 which generates an output signal that is applied to the input of bandlimiter 124. The output signal generated by the latter is then the conditioned sum signal.

[010] The difference channel processing section 130 receives the difference signal and generates the encoded difference signal. Section 130 includes a fixed preemphasis filter 132 (shown implemented as a cascade of two filters 132a and 132b), a variable gain amplifier 134 preferably in the form of a voltage-controlled amplifier, a variable preemphasis/deemphasis filter (referred to hereinafter as a "variable emphasis filter") 136, an overmodulation protector and bandlimiter 138, a fixed gain amplifier 140, a bandpass filter 142, an RMS level detector 144, a fixed gain amplifier 146, a bandpass filter 148, an RMS level detector 150, and a reciprocal generator 152. The processing of the difference signal ("L-R") by the section 130 is substantially as described in the Background section of U.S. Patent No. 5,796,842, which explains that the BTSC standard rigorously defines the desired operation of the 75 μ s preemphasis filter 122, the fixed preemphasis filter 132, the variable emphasis filter 136, and the bandpass filters 142, 148, in terms of idealized analog filters. Specifically, the BTSC standard provides a transfer

function for each of these components, and the transfer functions are described in terms of mathematical representations of idealized analog filters. The BTSC standard further defines the gain settings, Gain A and Gain B, of amplifiers 140 and 146, respectively, and also defines the operation of amplifier 134, RMS level detectors 144, 150, and reciprocal generator 152. The BTSC standard also provides suggested guidelines for the operation of overmodulation protector and bandlimiter 138 and bandlimiter 124. Specifically, bandlimiter 124 and the bandlimiter portion of overmodulation protector and bandlimiter 138 are described as low-pass filters with cutoff frequencies of 15 kHz, and the overmodulation protection portion of overmodulation protector and bandlimiter 138 is described as a threshold device that limits the amplitude of the encoded difference signal to 100% of full modulation where full modulation is the maximum permissible deviation level for modulating the audio subcarrier in a television signal.

[011] In the past, BTSC stereo encoders and decoders were implemented using analog circuits. Through careful calibration to tables and equations described in the BTSC standard, the encoders and decoders could be matched sufficiently to provide acceptable performance. However, conventional analog BTSC encoders (such as described in U.S. Patent No. 4,539,526) have been replaced by digital encoders because of the many benefits of digital technology. Prior attempts to implement the analog BTSC encoder 100 in digital form have failed to exactly match the performance of analog encoder 100. This difficulty arises from the fact that the BTSC standard defines all the critical components of idealized encoder 100 in terms of analog filter transfer functions, and prior digital encoders have not been able to provide digital filters that exactly match the requirements of the BTSC-specified analog filters. As a result, conventional digital BTSC encoders (such as those described in U.S. Patent Nos. 5, 796,842 and 6,118,879) have deviated from the theoretical ideal specified by the BTSC standard, and have attempted to compensate for this deviation by deliberately introducing a compensating phase or magnitude error in the encoding process.

[012] Given the processing capabilities of current signal processors, digital implementations of a BTSC encoder can result in the opposite problem of too much accuracy when the digital solution is capable of a far higher signal-to-noise ratio than the

analog solution. In this case, the digital encoder does not provide satisfactory performance in regions of operation where noise dominates the operation of the two feedback loops. This results in degradation in the performance of the encoding/decoding system and reduced stereo separation for the encoded signal.

[013] In addition to the complexity of the computational requirements for encoding the stereo signals, such as described above, the ever-increasing need for higher speed communications systems imposes additional performance requirements and resulting costs for BTSC encoding systems, such as where digital circuits requiring high speed clock rates are integrated on-chip with other digital circuits requiring different clock rates. In order to reduce costs, communications systems are increasingly implemented using Very Large Scale Integration (VLSI) techniques. The level of integration of communications systems is constantly increasing to take advantage of advances in integrated circuit manufacturing technology and the resulting cost reductions. This means that communications systems of higher and higher complexity are being implemented in a smaller and smaller number of integrated circuits. For reasons of cost and density of integration, the preferred technology is CMOS. To this end, digital signal processing ("DSP") techniques generally allow higher levels of complexity and easier scaling to finer geometry technologies than analog techniques, as well as superior testability and manufacturability.

[014] There is a need to provide a digital encoding system for processing stereophonic audio signals in compliance with an audio encoding standard that provides accurately encoded audio signals. Conventionally known systems have attempted to compensate for magnitude or phase errors created by imprecise digital filtering, or have suffered from degraded performance in low frequency operation where the digital encoder has a higher signal-to-noise ratio than the BTSC-specified analog decoder. Further, the nature of existing analog BTSC encoders has made them inconvenient to use with digital equipment such as digital playback devices. A digital BTSC encoder could accept the digital audio signals directly and could therefore be more easily integrated with other digital equipment. Therefore, there is a need for a better system that is capable of performing the above functions and overcoming these difficulties without increasing

circuit area and operational power. Further limitations and disadvantages of conventional systems will become apparent to one of skill in the art after reviewing the remainder of the present application with reference to the drawings and detailed description which follow.

SUMMARY OF THE INVENTION

[015] In accordance with the present invention, an integrated circuit system and method are provided for digitally encoding stereophonic audio signals in accordance with the BTSC standard. In a selected embodiment, an improved integrated circuit digital RF modulator system is provided with on-chip BTSC encoding functionality to support stereo transmission of audio to associated A/V components that have BTSC decoders. A digital, integrated circuit BTSC encoder and modulator eliminates the need for connecting line-level (RCA-type) audio connectors or an additional board of discrete analog components, to perform the modulation to provide the BTSC encoded RF output signal for use with a display device (television). A fully integrated solution that performs the RF modulation of the BTSC encoded output signal using digital techniques is provided.

[016] In a selected embodiment, a single chip set-top box integrated circuit is provided for encoding and modulating audio/visual signals. In the STB integrated circuit, a digital BTSC encoder encodes first and second digital audio signals (such as Pulse Code Modulation (PCM) baseband audio source signals) using a sum channel processor for digitally processing a digital sum signal and a difference channel processor for digitally processing a digital difference signal. The digital BTSC encoder operates at a sample rate of approximately at least ten times the bandwidth of the signal being encoded (for example, at least approximately 150-200 kHz in an audio encoding application) so that said digital filters in the sum channel processor and the difference channel processor substantially match BTSC analog filter transform functions in both magnitude and phase. The resulting BTSC encoded signal is RF modulated by a digital output modulator to generate a modulated output signal that is provided off chip, for example, as a channel 3/4 RF modulated audio/video signal for a display. In one embodiment, the digital output modulator is implemented as an audio/video processor that radio frequency (RF)

modulates an encoded audio/video signal to generate the modulated output signal. In an alternative embodiment, an audio signal is BTSC encoded and then processed by a rate converter and FM modulator to generate a processed audio signal that is combined with the processed video signal output from a video processor in an audio/video processor that combines the processed audio signal and the processed video signal into the audio/video signal. The digital output modulator may also include a Digital to Analog Converter (DAC) for transforming an audio/visual signal into an analog signal, where the DAC is clocked with a high speed clock signal whose timing relationship with the clock for the BTSC encoder is programmably controlled. The STB integrated circuit may be fabricated with CMOS processing technology so that the digital BTSC encoder and a digital output modulator are formed together on a common silicon substrate.

[017] With an alternative embodiment of the present invention, a method for modulating audio/visual signals on a single integrated circuit chip is provided, where audio data and video data is generated, encoded, processed, and modulated on the chip. In synchronization with the digital processing of video data to generate a composite video signal, an audio processor encodes the audio data using a BTSC encoder that operates with a sampling rate of at least of 200 kHz to generate a baseband BTSC composite signal. The baseband BTSC composite signal is rate converted from a first sampling rate to a second sampling rate on the chip, and is then used to frequency modulate an aural carrier using the converted baseband BTSC composite signal on the chip, thereby generating an FM modulated audio signal. By mixing the composite video signal and FM modulated audio signal to a programmable carrier frequency that may be chosen from 0 to 75 MHz, an RF modulated audio/visual signal is generated for output off chip to a display device as a channel 3/4 RF modulated audio/video signal.

[018] The objects, advantages and other novel features of the present invention will be apparent from the following detailed description when read in conjunction with the appended claims and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[019] FIG. 1 shows a block diagram of a prior art analog BTSC encoder.

[020] FIG. 2 depicts a system level description of a BTSC encoder.

[021] FIG. 3 depicts a block diagram of an alternate embodiment showing additional details of a BTSC encoder in accordance with the present invention.

[022] FIG. 4 is a system diagram illustrating an embodiment of an integrated all digital BTSC encoding RF modulator system built in accordance with the present invention.

[023] FIG. 5 is an overall block diagram illustrating an embodiment of a BTSC encoding RF modulator built in accordance with the present invention.

[024] FIG. 6 depicts an embodiment of a video processing path that is employed according to the present invention.

[025] FIG. 7 depicts a diagram illustrating an application of the present invention in the BTSC encoding RFM unit of a set-top box chip.

[026] FIG. 8 depicts a portion of an RFM clock generator.

DETAILED DESCRIPTION

[027] An apparatus and method in accordance with the present invention provide a system for digitally encoding stereo signals in accordance with the BTSC standard. A system level description of the operation of an embodiment of the BTSC encoder of the present invention is shown in Figure 2 which depicts a diagram of a digital BTSC encoder 200. As depicted in Figure 2, the output of encoder 200 is a BTSC compliant signal which includes stereo and SAP functionality for stereo encoding, advantageously sharing an amplitude/spectral compressor circuit 240 to thereby reduce the circuit size. It will be appreciated that the encoder of the present invention may also be implemented to provide the professional channel encoding specified by the BTSC standard, or may otherwise output a baseband BTSC multiplex signal at output 255. As will be appreciated, the BTSC encoder of the present invention has many potential applications. For example, the BTSC encoder may be included as part of an RF modulator core (RFM) in a television set-top box device that converts a NTSC/PAL/SECAM compliant digital composite video source and a pulse code modulated (PCM) audio source into an analog composite television signal that is suitable for demodulation by a television demodulator. A block diagram of an example is shown in Figure 7 (discussed below), which depicts an application of the present invention in the RFM unit of a set-top box chip. In this

application, the baseband BTSC composite signal 255 is fed to a rate converter and FM modulator that modulates the aural carrier, and the resulting signal is then summed with a baseband composite video signal. The combined audio/video signal is mixed to a RF frequency, converted to analog form and sent off chip.

[028] In connection with the system level description of Figure 2, when monophonic (MONO) audio processing is desired, the Left and Right channels of the input stereo audio signal 200, 202 are summed (in summer 212) and passed to a 75 μ second preemphasis filter 222. This datapath is considered to be the SUM channel. The 75 μ second preemphasis filter 222 provides extra gain to the high-frequency components. The output of the preemphasis filter 222 is passed directly to the summing device 250. The other two inputs to the final summation 250 in the BTSC encoder 200, which are the DIFF channel output 246 and the pilot tone 236, are zeroed out. Note that the SUM channel is sometimes referred to as the L+R channel, and the DIFF channel is sometimes referred to as the L-R channel.

[029] When SAP (secondary audio program) processing is desired in the encoder of Figure 2, the monophonic SAP signal replaces the "Right" audio input channel. The BTSC encoder first sharply bandlimits the SAP audio input stream to 10 kHz using a low-pass filter (not shown). The resulting signal is passed through the DIFF channel to a fixed preemphasis filter 232 whose characteristics are defined in the MTS OET-60. The output of this filter 232 is passed to amplitude/spectral compressor module 240. At modulator 242, the output of the amplitude/spectral compressor module 240 FM modulates the carrier sine wave whose frequency is five times the pilot rate of 15.734 kHz.

[030] When dual monophonic (DUAL MONO) operation is desired, a monophonic audio signal replaces the "Left" audio input channel, and the SAP signal replaces the "Right" audio input channel. Thus, the main monophonic signal is transmitted through the SUM channel at the same time that the SAP signal is transmitted through the DIFF channel. Multiplexer 245 is configured so that the SAP channel passes through the FM modulator 242. Note that in this case, the left audio input 200 and the

right SAP input 202 bypass the adder 212 and subtractor 214 and pass through the multiplexers 216 and 218 to the SUM channel and DIFF channel.

[031] Stereo processing is very similar to dual monophonic processing. In the encoder of Figure 2, an input section 210 receives the left and right channel audio input signals and generates therefrom a sum signal and a difference signal. A signal addition device 212 produces the SUM (L+R) channel based on the sum of the Left and Right channels of the input stereo audio signal. A signal subtraction device 214 produces the DIFF (L-R) channel based on the difference between the Left and Right channels of the input stereo audio signal. It will be appreciated that a matrix functionality may be used to receive the digital left and digital right signals and to generate the digital sum signal and digital difference signal. The SUM channel is passed through the 75 μ second preemphasis filter 222, and the DIFF channel is passed through the fixed preemphasis filter 232 and the amplitude/spectral compressor module 240. The output of amplitude/spectral compressor 240 is passed to the DSB SC (Double Side Band Suppressed Carrier) AM (Amplitude Modulator) block 244, where it amplitude modulates the sine wave carrier whose frequency (31,468 Hz) is equal to twice that of the pilot tone (15,734 Hz). The output 246 of this modulator along with 224 and 236 is passed to the sum block 250 that produces the BTSC composite signal 255. The output of encoder 200 is a BTSC composite signal 255 that is used to FM modulate the aural carrier.

[032] Figure 3 depicts a block diagram of an alternate embodiment showing additional details of an amplitude and spectral compressor. The difference channel processor consists of the fixed preemphasis filter 367, the compressor 301, and the right output filter 371 (e.g., a low pass Cauer filter). The compressor 301 is composed of the wideband gain loop and the spectral gain loop. The wideband gain loop is a loop formed by the following components: 306, 308, 371, and 340. The spectral gain loop is a loop formed by the components 308, 371, 320, and 322. The wideband RMS detectors 340 and the spectral RMS detectors 320 monitor the compressor output 352 and produce the wideband gain (WB GAIN 341) and the spectral gain (SP GAIN 321), respectively. The wideband gain is used to control the wideband amplifier 306, which is essentially a

divider. Using a clamp or saturator in the WB gain path (e.g., in block 339), the feedback input 341 to the divider 306 is saturated to a minimum value (depending upon the sign of the input) if the wideband gain reaches a minimum threshold value. A similar clamping technique may be used in the spectral gain loop to control the spectral gain value (SP GAIN 321) that is used to compute the coefficients of the spectral compressor 308 using the coefficient calculator 322, on-the-fly. Three divide operations are required to calculate the coefficients and these are also performed on-the-fly in the coefficient calculator 322.

[033] Another way of viewing the difference channel processor shown in Figure 3 is that the amplitude/spectral compressor module 301 is essentially a wideband gain stage 306 that is followed by a variable preemphasis filter, or spectral compressor, 308. The wideband gain stage 306 is controlled by the WB GAIN signal 341 through the wideband gain loop or feedback path. The spectral compressor 308 is controlled by the SP GAIN signal 321 through the spectral gain loop or feedback path. As depicted, the feedback paths of the BTSC encoder begin at the output 352 of the right low-pass Cauer filter ROCF 371. These feedback paths are used to control the wideband divider 306 and spectral compressor 308. The spectral feedback path control signal is based on the RMS power that passes through a bandpass filter 314 with a 10 kHz center frequency. The wideband feedback path control signal is based on the RMS power that passes through a bandpass filter 334 with a 2 kHz center frequency. When the input signal to the BTSC encoder is a low frequency signal, the feedback paths are dominated by noise because the signal lies outside the passband of the bandpass filters 314, 334.

[034] As indicated in Figure 3, the BTSC encoder receives two audio channel inputs (L 303 and R 305). To allow proper digital processing of the signals, the encoder should operate at a sufficiently high rate (for example, 10-20 times the audio bandwidth) to allow the analog and digital filters to match in phase and amplitude. The choice of the sampling rate is driven by the need for the digital filter implementations to more closely match the analog filter transform functions (specified by the BTSC standard) in both magnitude and phase. A sample rate of 316 kHz results in good matching of the magnitude and phase responses between the analog and digital domains so that no phase

compensation is needed in the encoding process. In a selected embodiment, two channel inputs 303, 305 which arrive at a first sample rate (e.g., 27 Mhz/32) are converted to a second sample rate (e.g., 54 MHz/171) by the input VIDs (Variable Rate Interpolator Decimator) 300.

[035] The input streams to the encoder are filtered by low-pass Cauer filters 302 to limit the bandwidth of signals for system compliance. For MONO mode of operation (with stereo and SAP turned off), the two audio inputs may be programmably limited to 15-20 kHz or to other frequencies. For STEREO mode of operation, the two audio inputs are limited to 15 kHz. For MONO/SAP mode of operation, the input 303 for audio channel 1 is limited to 15 kHz while the input 305 for audio channel 2 is limited to 10 kHz. This low-pass filtering operation is achieved by reprogramming the coefficients to the input low-pass Cauer filters 302 for each mode of operation. By designing the input low-pass Cauer filters 302 to have sharp transition bands, emphasis of noise outside of the audio bands is prevented during the encoding operation. By providing input filters with stop-band attenuation of -70dB, good rejection of the input out-of-band noise after the preemphasis is provided.

[036] In the encoding system, output low-pass Cauer filters 370 and 371 reduce the high-frequency out-of-band noise that is amplified by the filters 366, 367, 306 and 308. The resulting filtered digital sum signal 350 and filtered digital difference signal 352 may be processed, programmably scaled and clipped in the modulator block 354. Modulator 354 is used to inject the pilot subcarrier that is frequency locked to the horizontal scanning frequency of the transmitted video signal, as required by the MTS OET-60 standard. In addition, AM-DSB-SC or FM modulation may be implemented in modulator 354 for modulating the digital difference signal 352.

[037] As referenced above, the BTSC encoder of the present invention may be included in a variety of applications, such as the RF Modulator core 42 shown in Figure 4, which illustrates an embodiment of an integrated all digital BTSC encoding RF modulator system built in accordance with the present invention. A Set Top Box (STB) 40 interfaces with audio/video devices, such as legacy television display 47 or a baseband digital display 48. A single integrated circuit 40 supports the functionality of the STB,

including the functionality of the invention of including an integrated, all digital RF modulator and BTSC encoder 42.

[038] The legacy display 47 requires the use of a Radio Frequency (RF) input signal 44 (that may be referred to as an RF modulator output signal from the perspective of the STB 40). This RF modulated output signal 44 may be implemented as being a channel 3/4 (or such) RF modulated audio/video signal in some embodiments for compatibility with the assigned Channel 3 or Channel 4 Radio Frequencies (RFs). While the receiver module 47 is typically a display device, the receiver module may also include non-display audio/video (A/V) devices that are able to receive the RF modulator output signal, such as a Video Cassette Recorder (VCR) 49 or some other type of intermediary device.

[039] The STB 40 includes an all digital RF modulator 42 that is able to generate the RF modulator output signal that is required as an input to the legacy display. The RF modulator 42 can also generate RF-modulated input signals onto television channels other than channels 2-4. In addition, an unmodulated baseband BTSC composite signal may be directly passed to output. The all digital RF modulator 42 may be viewed as being an integrated circuit Digital Signal Processor (DSP) functional block which includes a BTSC encoding functionality. The legacy display 47 includes a RF input signal interface 46 that is able to receive the RF modulator output signal 44 from the all digital RF modulator 42 of the STB 40. The input signal interface 46 may also include a BTSC decoder functionality for decoding BTSC encoded signals. The legacy display 47 may be viewed as being an older television (TV) model, or any other display, that may receive an RF input. In a display device that includes functionality for both baseband inputs as well as RF-modulated inputs, there may be times when the RF input may be preferred. Either of the outputs from the STB 40 may be selected. The present invention shows, for the first time, a fully integrated BTSC encoder and RF modulator 42 that may be implemented in CMOS (Complementary Metal Oxide Semiconductor), as part of a single chip STB 40. In other words, an integrated circuit that includes the STB functionality may be fabricated using CMOS (Complementary Metal Oxide Semiconductor) processing.

[040] The present invention allows for backward compatibility with the number of legacy displays that are still in use today. A video encoder 43 and an audio source 41 are operable to provide digital signals to the all digital RF modulator 42 within the STB 40, so that the all digital RF modulator 42 may generate the appropriate encoded RF modulator output signal for use with the audio/video devices.

[041] In accordance with the present invention, the STB 40 also includes the ability to provide composite, S-video, and/or component video (for example, red/green/blue or RGB) outputs 45 for use within a baseband display 48. The video encoder 43 (with its Digital to Analog Converters (DACs)) produces a signal that may be in one of these formats for output to the baseband display 48. The baseband display 48 may include a number of devices such as a High Definition Television (HDTV), a computer, or other display that may accept as input a signal in one or more formats. Composite video, S-video, and/or component video are illustrative of some of the many types of signals that may be provided by the STB 40 to the baseband display 48. It is also noted that the display 48, if equipped with a RF modulated analog input port, would also be capable of receiving the RF modulator output 44 as well.

[042] Persons skilled in the art will appreciate that an RF modulator is not a rigidly defined concept, and can be understood to refer to a specific rate conversion, amplitude modulation and/or frequency modulation functions, or more broadly to a signal processing, conditioning and/or encoding function in combination with a sampling rate conversion, amplitude modulation and/or frequency modulation. For example and as illustrated in Figure 5, an embodiment of an RF modulator built in accordance with the present invention includes a video processor 51, audio processor 55 and audio/video processor 52, and the collection of these blocks provides BTSC encoding, rate conversion, amplitude modulation and frequency modulation. Video processor 51 receives the composite video signal 50 and, after video processing, provides an output to an audio/video processor 52. Audio processor 55 receives audio signals 53, 54 and, after audio processing, provides an output to the audio/video processor 52. The audio/video processor 52 provides an off chip signal 59. The RF modulator also includes a clock

generator 56, a local bus interface 57 and a test control portion 58 that supports additional corresponding functionality.

[043] As illustrated in Figure 5, the RF modulator receives a composite video input signal 50 and one or more baseband audio source input signals 53 (such as PCM (Pulse Code Modulation) audio data) and/or an audio “multiplex” signal 54 (such as BTSC (Broadcast Television Systems Committee) audio data). In the RF modulator, the baseband video signal 50 is first filtered to pre-compensate for the group delay distortion in the receiver. Then, the video is filtered to remove any signal components in the audio carrier frequency band. The signal is then scaled and shifted to meet the depth of modulation requirements. In the audio/video processor 52, the frequency modulated (FM) audio signal is added to the video signal. The sum (audio + video) signal is then sample rate converted to a high frequency sample rate. The signal is then modulated to the desired RF frequency.

[044] Figure 6 illustrates additional details of the video processing path in accordance with the present invention. As depicted, composite video signal 60 is provided to an asynchronous FIFO (First In/First Out) device 61 that operates at 27 MHz. Then, the output signal of the asynchronous FIFO 61 is decimated by a factor of 2 in downsampling filter 62 which reduces the sampling rate from 27 MHz to 13.5 MHz. Then, a programmable group delay digital filter 63 compensates the decimated output signal for the specific group delay requirements. An audio trap digital filter 64 attenuates video components in the audio carrier frequency band, and is operable to attenuate video signals in a frequency range of an audio signal that contains an audio FM (Frequency Modulated) carrier. This audio signal may be either one or both of a baseband audio signal and/or an audio multiplex signal that FM modulates the audio carrier. A pilot control block 65 provides an output signal 66 to an A/V (Audio/Video) processor. For example, the video processing path may be viewed as being performed within the video processor 51 to provide an output signal 66 to an A/V processor 52, as shown in Figure 5.

[045] The preceding and following figures described herein provide illustrative examples of the various frequencies at which a device operating in accordance with the invention may operate. It will be understood that the particular values shown herein may

be altered without departing from the scope and spirit of the invention; these particular values are exemplary of just some of the possible embodiments in which the invention may be implemented.

[046] As referenced above, the BTSC encoder of the present invention may be included in a variety of applications, such as the RF Modulator core (RFM 414) depicted in Figure 7 for generating the RF TV composite signal that is used by a set-top box to generate channel 3/4 output signal(s) 427. In the depicted embodiment, RFM 414 converts a NTSC/PAL/SECAM compliant digital composite video source 434 and a pulse code modulated (PCM) audio source 411a, 411b into an analog composite television signal 427 that is suitable for demodulation by a television demodulator. Moreover, the RFM 414 may stereo encode the audio source according to the BTSC standard. In a single chip integrated circuit embodiment of the present invention, a digital BTSC encoder 416 is disclosed for encoding stereo audio signals 411, where the encoder 416 is integrated as part of a single chip set-top box 400 fabricated with CMOS technology. Upon integration into a set-top box chip 400, the present invention reduces board level components, thereby reducing costs and improving performance over prior art approaches. Thus, the present invention shows, for the first time, a fully integrated digital BTSC encoder 416 that may be implemented in CMOS as part of a single chip set-top box 400.

[047] The block diagram in Figure 7 shows the various operations to be performed in the RFM 414, as well as the primary datapath input and output signals. As depicted in the context of a set-top box chip shown in Figure 7, the RFM 414 can be considered to be a part of the audio/video back end. A simplified drawing of part of a set-top box is depicted in Figure 7 with a focus on the operations performed for an analog television channel. For additional contextual understanding of how the present invention may be implemented in various illustrative set top box embodiments, see the description of Figures 6, 7 and 8 provided in co-pending U.S. patent application no. 10/372,427, entitled "All Digital Radio Frequency Modulator," filed February 21, 2003, and assigned to Broadcom Corporation, which is hereby incorporated by reference in its entirety. In accordance with the present invention, the BTSC encoding functionality may be

implemented as an integral part of the RF modulator block described in the foregoing application.

[048] In a further application of the present invention, a dual high-definition (HD) digital video system-on-a-chip includes BTSC encoding circuitry, RF modulation circuitry and dual digital audio processors for processing multiple audio/video programs. The system-on-a-chip may include an IF demodulator, an NTSC/PAL video decoder, a transport processor, dual digital audio processors, dual high-definition (HD) MPEG video decoders, 2D and 3D graphics processing, digital processing of analog video and audio, an analog video digitizer and DAC functions (six DACs), stereo high-fidelity audio DACs, a MIPS R5000 class processor, and a peripheral control unit providing a variety of set-top box control functions.

[049] In a selected embodiment depicted in Figure 7, the set-top box chip may contain blocks that perform the inverse functions to the RFM. Thus, an IF demodulator ("IFDEMODO") block 402 demodulates an analog composite IF television signal and produces a digital baseband composite video signal 405 and a digital baseband audio signal 403 (either monophonic or BTSC baseband multiplex). By exchanging data between the RFM 414 and IFDEMODO 402, both can be co-verified on the system bench using an all-digital interface. This exchange of data is referred to as a "loopback mode" and may be used for test functions. The purpose of the loopback mode from the IFDEMODO 410 to the RFM 414 is to allow the audio and video data that is associated with an analog television channel to "pass through" the chip without requiring any encoding or decoding.

[050] The primary audio source for the RFM 414 is the stereo high fidelity audio DAC 410 (HiFiDAC) that is part of the audio processor 406. As shown, BTSC decoder 404 receives the baseband composite audio signal 403 and generates a decoded audio signal for the audio processor 406. HiFiDAC 410 provides two channels (411a, 411b) of pulse code modulated (PCM) audio data to the RFM 414. The primary video source for the RFM 414 is the video encoder 430 (VEC) which receives digital video stream data from the video decoder 428. VEC 430 provides the NTSC, PAL, or SECAM encoded digital baseband composite video signal 434 that accompanies the HiFiDAC's audio

signal. VEC 430 also provides a video start-of-line signal 431 that allows the RFM to lock its audio subcarriers to the video line rate. In accordance with the present invention, one or more VECs are provided, depending on how many output channels are supported by the STB.

[051] In terms of the audio/video backend functionality of the set-top box chip 400, the RFM 414 includes a digital audio processor portion (416, 418), a digital video processor portion (420) and a digital audio/video processor portion (422, 424, 426). The digital audio processor portion includes the BTSC encoder 416 and rate converter with FM modulator 418. The RFM 414 accepts four input signals, including three input signals for the BTSC encoder 416 which are expected to be employed in normal operation and a baseband composite video input signal 434. The first two BTSC encoder input signals are two channels of audio PCM data 411a, 411b. The third BTSC encoder input signal is the video start-of-line signal 431, which is used to synchronize the pilot tone needed for BTSC encoding to the video line rate. The BTSC encoded audio is combined with the video data at adder 422 at the digital audio/video processor and then rate converted, mixed to RF (424) and converted from digital to analog format (426) to generate the RF TV composite output signal 427. In a selected embodiment, the digital video 421 and FM modulated audio 419 signals are converted and mixed at block 424 to a programmable carrier frequency that may be chosen from 0 to 75 MHz, which includes NTSC channels 2, 3 and 4. In order to maintain reasonable separation of the spectral images in the analog output of the digital-to-analog converter, the DAC 426 is clocked with as high a clock rate as possible.

[052] As will be appreciated, the audio processing path depicted in Figure 7 shows that two channels of PCM audio signals 411 are provided to the BTSC encoder 416 where they are encoded into sum and difference channels. An asynchronous capture functional block may be provided in the RFM 414 to operate at a programmable audio-range sample rate (for example, 48 kHz in one embodiment) to capture the audio input signals 411, and a variable interpolator decimator (VID) converts the signal to a desired sample rate. Alternatively, a synchronous capture function block and VID may be provided in the RFM 414 to convert the sampling rate of the audio input signals 411. The

BTSC encoder 416 operates at a predetermined sample rate and provides an encoded audio output to a VID rate converter 418 that changes the sample rate (e.g., to 27 MHz) and then frequency modulates the signal.

[053] With the present invention, other types of audio input signals could be provided to the audio processor 416, 418 for capture, rate conversion and FM modulation. For example, a BTSC multiplex audio signal may be scaled, captured by an asynchronous FIFO operating at 316 kHz, asynchronously rate converted from 316 kHz to 27 MHz, and then multiplexed or directly input to an FM modulator circuit prior to output to the A/V processor.

[054] In accordance with the present invention, the digital video processor 420 receives as a video input a digital video composite signal 434 that contains the full NTSC, PAL, or SECAM encoded signal. In a selected embodiment, a selectable or programmable audio trap filter is provided in the form of a lowpass filter to reduce video signal content at the audio carrier frequencies. In addition, a programmable group delay digital filter may be provided to compensate the decimated output signal for the specific group delay requirements.

[055] As depicted in Figure 7, the digital audio/video processor portion of the RFM 414 includes a summer 422, rate converter/mixer 424 and DAC 426. Rate converter/mixer 424 may be implemented with an upsample block and modulator that receives the combined video and audio input signal from summer 422 and interpolates that signal by a factor of 4, from 27 MHz to 108 MHz. In addition, rate converter/mixer 424 may change the data sample rate from 108 MHz to 405 MHz, for example. In the rate converter/mixer 424, the output of a sine generator operating at 405 MHz (not shown) is mixed or combined with the output from the rate converter and provided to an $x/\sin(x)$ digital filter (not shown) before being converted to analog form by DAC 426. Thus, the signal provided to the DAC 426 is filtered to compensate for $\sin X/X$ distortion inherent in the digital to analog conversion process. The output 427 of the DAC 426 may then be provided off chip. Though not illustrated in Figure 7, an analog PLL (Phase Locked Loop) circuit clocked with a reference signal (e.g., 27 MHz or 54 MHz) provides an output signal of 405 MHz to the DAC 426.

[056] As shown in Figure 7, the final stage of the RFM 414 is the digital-to-analog converter 426. DAC 426 is clocked at very high speeds (up to 405 MHz) to move spectral images as far apart as possible. In order to prevent analog performance degradation, DAC 426 is clocked by a very low-jitter clock that is provided by an analog phase locked loop (PLL) illustrated in Figure 8.

[057] As illustrated in Figure 8, which shows a portion of the high speed RFM clock generator, PLL 802 is sourced by a 54 MHz differential clock 801 provided by an overtone oscillator (not shown). (Persons skilled in the art will recognize that only selected output buffering stage elements of the PLL are depicted in Figure 8, and that the PLL can be implemented as a digital PLL or analog PLL circuit.) The PLL 802 outputs a clock signal 803 (aclko) that is used to clock the RFM DAC 426, but also outputs another clock signal 804 (dclko) that is used to derive other clocks used internally within the RFM 414. Figure 8 shows an example circuitry for high speed clock generation. As depicted, PLL 802 provides the capability to select the phase of the aclko clock signal 803 such that it balances with clock 2. This allows a straightforward handoff from the digital logic in the RFM 414 to the DAC 426.

[058] In particular, the high speed DAC interface requires careful clock balancing. As described herein, DAC 426 requires a jitter-free clock in order to prevent analog performance degradation. Thus, the analog clock output 803 (aclko) from PLL 802 is routed directly to DAC 426 and does not traverse any digital cells. However, the digital clock output 804 (dclko) of the PLL 802 traverses digital delay elements, such as a clock tree 806. Accordingly, a timing skew is introduced between the clocks that drive the RFM's digital section and the clock that drives DAC 426. In a selected embodiment, the clock skew is reduced with a programmable delay line in PLL 802. As illustrated in Figure 8, the inserted delay is a series of inverter or delay elements 805 that are controlled through the phase control signal 807. The aclko and dclko propagation delays through the PLL 802 are characterized so that the handoff from the RFM output registers to the DAC can be analyzed prior to tapeout using standard static timing methodologies.

[059] Benefits of the clocking scheme depicted in Figure 8 are flexibility, portability, and good control over clock skews. However, the PLL's output clocks (aclko

and dclko) that are used by the RFM 414 are inherently asynchronous relative to the output clocks from the chip's system PLL. In order to alleviate the burden on other blocks, asynchronous FIFO interfaces may be provided in the RFM 414 that allow it to communicate synchronously with all other blocks on the chip using a system clock that is derived from the chip's system PLL. Because the PLL 802 and the system PLL are both driven by the same crystal, they should be frequency locked.

[060] In an alternative embodiment, the clocking of the digital logic of the RF modulator may be implemented using the clock synchronization loop described in connection with co-pending U.S. patent application no. 10/372,427, entitled "All Digital Radio Frequency Modulator," filed February 21, 2003, and assigned to Broadcom Corporation, which is hereby incorporated by reference in its entirety. In connection with the synchronization loop illustrated in Figure 9 of this incorporated application, synchronous and asynchronous clocking modes are provided. In this context, synchronous clocking implies a frequency lock (or known frequency relationship) between the chip's system PLL and the RFM PLL, and asynchronous clocking implies there is no frequency lock (or no known frequency relationship) between the PLLs. The synchronization loop handles the disparity in the asynchronous clocking mode.

[061] Referring back to Figure 3, because analog and digital circuits fundamentally have different noise characteristics, the low frequency stereo separation for a digital encoder and an analog decoder can be substantially improved by adjusting the spectral gain 321, which is the control signal that is input to the spectral compressor's coefficient calculator 322. These adjustments are designed to account for the increased noise that is typically found in an analog system relative to a digital system, and can substantially improve the low frequency stereo separation for a digital encoder and an analog decoder. As will be appreciated, the adjustments to the control signal can be performed by spectral compressor's coefficient calculator 322, or can be implemented by other adjustment circuitry in the feedback path connected to the input of the spectral compressor 308 or calculator 321. These adjustments are designed to account for differing amounts of noise energy found in an analog system relative to a digital system. The SP GAIN 321 (as well as the WB GAIN 341) is the exponentially time-weighted

root-mean-square value of the signal energy found in a particular band of audio frequencies. In the lower frequency band (i.e., below 2 kHz), the signal energy is comparable to the noise energy. As a result, the contributions by the noise energy to SP GAIN 321, when compared with the signal energy, are significant. Therefore, any difference in the noise characteristics between an encoder and a decoder can result in differing values for the computed SP GAIN 321. This mismatch leads to degraded stereo separation.

[062] In accordance with the present invention, stereo separation at low frequencies can be improved by selectively adjusting the SP GAIN signal 321, using a variety of techniques such as described herein. In one embodiment, a clamp or saturator is used in the wideband or spectral gain feedback path to prevent the gain control signal from going below a minimum value. In another embodiment, a minor or adjustable offset is added to the spectral gain only if the spectral gain is below a certain threshold or comparison point. With this offset, stereo separation is improved for most frequencies. However, minor stereo separation jitter appears at the frequencies where the spectral gain oscillates about the maximum comparison point. Such jitter can be in terms of minor amplitude and phase variation for a single frequency. An alternative embodiment of the present invention helps control the jitter in the separation by rolling off or tapering the offset value when the spectral gain is above a maximum comparison point. Tapering the offset addresses the situation where the comparator is injecting a value of spectral gain that is noisy and that fluctuates about a comparison point for a single tone going through the compressor. Techniques for adjusting the spectral gain (SP GAIN 321) and/or the wideband gain signal (WB GAIN 341) can be implemented as described in the co-pending U.S. patent application entitled "Mechanism For Using Clamping And Offset Techniques To Adjust The Spectral And Wideband Gains In The Feedback Loops Of A BTSC Encoder," filed _____, and assigned to Broadcom Corporation, which is hereby incorporated by reference in its entirety to provide detailed information about the control signal adjustment techniques.

[063] The datapath outputs from RFM 414 are the differential outputs from DAC 426. These analog signals contain the RFM A/V composite signals that are routed

to the chip pins. The audio/video composite signal is typically modulated to NTSC Channel 3 (61.25 MHz) or NTSC Channel 4 (67.25 MHz). In order to maintain reasonable separation between the DAC images, DAC 426 is clocked with as high a clock rate as possible.

[064] As will be appreciated, a selected embodiment of the present invention provides for proper digital processing of the signals by utilizing a BTSC encoder that operates at a minimum rate of about ten times the signal bandwidth, e.g., 150-200 kHz. Lower or higher sampling rates can be used, provided that good matching is achieved between the analog and digital filter performance requirements. In particular, the choice of the sampling rate is driven by the need for the digital filter implementations to more closely match the analog filter transform functions (specified by the BTSC standard) in both magnitude and phase. By implementing a BTSC encoder with a programmable sampling rate, lower sampling rates can be used in applications where lower performance is acceptable.

[065] While the system and method of the present invention has been described in connection with the preferred embodiment, it is not intended to limit the invention to the particular form set forth, but on the contrary, is intended to cover such alternatives, modifications and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims so that those skilled in the art should understand that they can make various changes, substitutions and alterations without departing from the spirit and scope of the invention in its broadest form.